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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,693	04/04/2001	Mario Nemirovsky	P3819	4332

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,693	NEMIROVSKY ET AL.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006 and 27 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statements received 21 April 2005, 16 June 2005, 11 September 2005, 02 October 2005, 21 October 2005, 20 November 2005, 27 November 2005, 13 December 2005, and 20 December 2005 have been considered except as noted below. Please see the attached PTO-1449(s).

2. On the IDS received 21 April 2005, U.S. Patent Application Serial number 09/608,750 should be listed under the "Non-patent Literature" section (see MPEP 609.04(a)(I)). The information has been considered and added to the attached PTO-892.

3. On the IDS received 21 April 2005, document "AP" to "Kessler et al." has not been considered because the copy of the document received is not legible. See 37 CFR 1.98(a)(2)(ii) and MPEP 609.04(a)(II).

4. On the IDS received 16 June 2005, U.S. Patent Application Serial number 09/602,279 should be listed under the "Non-patent Literature" section (see MPEP 609.04(a)(I)). The information has been considered and added to the NPL section of the 16 June 2005 IDS.

5. On the IDS received 21 October 2005, U.S. Patent Application Serial number 09/591,510 should be listed under the "Non-patent Literature" section (see MPEP 609.04(a)(I)). The information has been considered and added to the attached PTO-892.

Claim Objections

6. Claims 3-4 and 14-17 are objected to because of the following informalities:

As per claim 3, line 27, "within said data cache" should be deleted based on Applicant's amendment to claim 3, line 17.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-6, 10, 12-13, and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey et al. (5,724,565) in view of Meier (6,523,109) and Anderson et al. (5,951,679).

As per claim 1, 3, and 5, Dubey et al. teaches a central processing unit ("microprocessor") for processing multiple parallel instruction threads ("instruction streams"). The CPU includes a plurality of instruction buffers 141 (figure 1; "instruction queues") which correspond to the multiple threads. See column 6, line 67, to column 7, line 2, and column 7, lines 55-61. The CPU includes one or more functional units (see column 6, lines 24-26) and a data cache (see column 6, line 49). Dubey et al. teaches different types of instructions, including branch instructions ("first instructions", noting that Dubey et al. teaches that a branch unit is a type of functional unit; see column 1, lines 23-26 and 57-59), load instructions (column 28, line

23), and store instructions (column 28, lines 22-23). Dubey et al. also suggests a store queue ("bypass structure") and resolving memory dependencies between loads and stores. See column 28, lines 19-26.

Dubey et al. does not teach address matching logic and switching logic in association with the store queue ("bypass structure").

Meier teaches a store queue 68 (figures 3-4) for a data cache 44 (figure 1). The store queue includes a plurality of entries ("bypass structure...for receiving said store instructions...comprising multiple elements"). See figure 4. A comparison between a load address and entries in the store buffer is performed by a store queue number assignment circuit 60 ("address matching logic...for receiving load instructions..."). See column 10, lines 62-64, and column 11, lines 11-13 and 43-54. Meier teaches a merge/align circuit 120 in the data cache for merging bytes from the store queue with bytes from the data cache ("switching logic"). See column 18, lines 26-32. Meier also teaches that load (read) operation may match on multiple elements in the store queue ("wherein one of said read operations matches on multiple elements of said bypass structure", claim 3). See column 2, lines 20-23.

It would have been obvious to one of ordinary skill in the art to have modified the store queue of Dubey et al. to include the address matching and switching logic suggested by Meier (detailed above), because Meier teaches that such a store buffer implementation would conserve the amount of circuitry used and decreases average load latency (see column 1, lines 52-55 and 66-67), as well as optimizing code sequences (column 2, lines 27-32).

Furthermore, the combination of Dubey et al. and Meier does not teach read and write pointers and retaining up to 8 instructions already dispatched so that they can be dispatched

again in the case that a short backward branch is encountered. Anderson et al. teaches a queue in a superscalar system including a top pointer ("read pointer"; column 15, lines 15-17), a bottom pointer ("write pointer"; column 15, lines 17-19), and maintaining 5 instruction in the queue for short backward branches (see column 3, lines 3-12). It would have been obvious to one of ordinary skill in the art to have modified the queues of the combination of Dubey et al. and Meier to include read and write pointers and store instructions for short backward branches, as suggested by Anderson et al., because this would allow the microprocessor to operate more efficiently (see column 2, lines 60-63).

As per claims 2, 4, and 6, Meier teaches that the store buffer stores a quadword ("32 bits") of data per entry. See column 15, lines 35-36, and as shown in figure 4, there are more than 6 entries in the buffer ("comprising... six elements").

As per claim 10, Dubey et al. teaches that the data cache 170 is multi-ported (wherein "multi-port" may only be two ports). See column 9, lines 4-7.

As per claims 12 and 22, Meier teaches a multi-match condition where the youngest (i.e. "newest version") is selected from the store queue on a load (read) hit. See column 19, line 64, to column 20, line 9.

As per claims 13 and 23, Meier teaches a merge/align circuit 120 in the data cache for merging bytes from the store queue with bytes from the data cache. See column 18, lines 26-32.

9. Claims 7-9, 11, 14-17, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubey et al. in view of Meier and Anderson et al. in further view of Levy et al. (U.S. 2001/0004755).

As per claims 7, 14, and 18, it is noted that Dubey et al. has a number of instruction buffers that equals the number of threads that are executing simultaneously. See figure 1 and corresponding description. The combination of Dubey et al., Meier, and Anderson et al. does not teach eight instruction buffers ("queues"), each corresponding to eight instruction threads ("streams"). Levy et al. teaches a processor executing a maximum of eight threads simultaneously. See page 7, paragraph [0085], line 7. It would have been obvious to one of ordinary skill in the art to have implemented 8 instruction buffer for 8 threads in the system of Dubey et al., as suggested by Levy et al., because Levy et al. teaches that with 8 threads stalling drops and provides the greatest choice of instructions to issue. See page 7, paragraph [0085], lines 7-10.

As per claims 8, 15, and 19, Dubey et al. teaches that the data cache 170 is multi-ported (wherein "multi-port" may only be two ports). See column 9, lines 4-7. If the cache memory only has two ports, then a maximum of two read (load) operations may be performed in on cycle on the data cache memory.

As per claims 9, 16, and 20, Dubey et al. teaches that the data cache 170 is multi-ported (wherein "multi-port" may only be two ports). See column 9, lines 4-7. If the cache memory only has two ports, then a maximum of two write (store) operations may be performed in on cycle on the data cache memory.

As per claims 11, 17, and 21, the combination of Dubey et al., Meier, and Anderson et al. does not teach that the threads are based on the MIPS instruction set architecture. Levy et al. teaches that it was know to utilize a MIPS instruction set processor in a multithreading system. See page 8, paragraph [0092]. It would have been obvious to have utilized a MIPS instruction

set with the simultaneous multithreaded system of the combination of Dubey et al. and Meier because the MIPS architecture boosts programming performance by using an out-of-order instruction execution. See Levy et al, page 4, paragraph [0052].

Response to Arguments

10. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's amendments to the claims.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks

Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(571) 273-8300**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2185

RGB
January 22, 2006